4. (original) The integrated circuit timing circuit of claim 1 further comprises a set/reset latch coupled to an output of the adjustable delay element.

5. (original) The integrated circuit timing circuit of claim 1 wherein the adjustable delay element comprises a plurality of capacitors selectively coupled to a propagation path in response to the programmable non-volatile fuse circuit to establish one of the plurality of propagation times.

6. (currently amended) An integrated circuit timing circuit comprising:

a programmable non-volatile fuse circuit;

a volatile latch circuit coupled to the non-volatile fuse circuit; and

a plurality of adjustable delay elements generating a signal having an edge, each adjustable delay element coupled to the volatile latch circuit, each of the plurality of adjustable delay elements comprises a propagation path, and a plurality of capacitors selectively coupled to the propagation paths of the plurality of adjustable delay elements in response to the volatile latch circuit; and

a plurality of set/reset flip-flops triggered off of a signal edge or a certain number of delay elements and reset by other edges or numbers of delay elements.

7. (original) The integrated circuit timing circuit of claim 6 wherein the plurality of capacitors selectively coupled to the propagation paths via a switch activated by the volatile latch circuit.

8. (original) The integrated circuit timing circuit of claim 6 further comprising:

logic circuitry coupled to an input of the plurality of adjustable delay elements; and

latch circuitry coupled to an output of the plurality of adjustable delay elements.

9. (currently amended) A memory device comprising:

an array of memory cells;

access circuitry to generate a plurality of memory array access signals; and

an adjustable timing circuit coupled to the access circuitry, the adjustable timing circuit comprises,

a programmable non-volatile fuse circuit, and

an adjustable delay element coupled to the programmable non-volatile fuse circuit, the delay element has a plurality of propagation times selectable in response to the programmable non-volatile fuse circuit, the delay element to adjust one of an edge position of at least one signal relative to other edges, a plurality of edge positions relative to other edges, or a duration of a single signal relative to other signals.

10. (original) The memory device of claim 9 further comprising a volatile latch circuit coupled between the programmable non-volatile fuse circuit and the adjustable delay element.

11. (original) The memory device of claim 9 wherein the programmable non-volatile fuse circuit comprises a plurality of flash memory cells.

12. (original) The memory device of claim 9 wherein the adjustable delay element comprises a plurality of capacitors selectively coupled to a propagation path in response to the programmable non-volatile fuse circuit to establish one of the plurality of propagation times.

13. (currently amended) A synchronous flash memory device comprising:

an array of non-volatile memory cells;

access circuitry to generate a plurality of memory array access signals; and

an adjustable timing circuit coupled to the access circuitry, the adjustable timing circuit comprises,

a programmable non-volatile fuse circuit comprising non-volatile memory cells,

a volatile latch circuit coupled to the non-volatile fuse circuit, and

a plurality of adjustable delay elements generating a signal having an edge, each adjustable delay element coupled to the volatile latch circuit, each of the plurality of adjustable delay elements comprises a propagation path, and a plurality of capacitors selectively coupled to the propagation paths of the plurality of adjustable delay elements in response to the volatile latch circuit; and

a plurality of set/reset flip-flops triggered off of a signal edge or a certain number of delay elements and reset by other edges or numbers of delay elements.

14. (original) The flash memory of claim 13 wherein the plurality of capacitors selectively coupled to the propagation paths via a switch activated by the volatile latch circuit.

15. (currently amended) A method of adjusting a signal timing circuit comprising:

programming a non-volatile fuse circuit; ~~and~~

selecting a signal propagation time length in response to the programmed non-volatile fuse circuit; and

selecting an edge position in response to the programmed non-volatile fuse circuit.

16. (original) The method of claim 15 wherein selecting the signal propagation time length comprises selectively coupling one or more capacitors to a propagation path of the signal timing circuit.

17. (original) The method of claim 15 wherein the non-volatile fuse circuit comprises a plurality of floating gate transistors.

18. (original) The method of claim 15 further comprises storing data from the non-volatile fuse circuit in a plurality of volatile latches.

19. (currently amended) A method of adjusting a signal timing circuit comprising:

programming a plurality of non-volatile fuses to store first data;

copying the first data from the plurality of non-volatile fuses to a plurality of latch circuits; ~~and~~

selecting a signal propagation time length in response to the first data stored in the plurality of latch circuits; and

selecting an edge position in response to the programmed non-volatile fuse circuit.

20. (original) The method of claim 19 wherein the wherein selecting the signal propagation time length comprises selectively coupling one or more capacitors to a propagation path of the signal timing circuit.

21. (original) The method of claim 19 wherein the non-volatile fuse circuit comprises a plurality of floating gate transistors.

22. (currently amended) A method of testing a memory device comprising a signal propagation path, the method comprises:

programming a plurality of non-volatile fuses to store first data;

selectively coupling one or more capacitors to the propagation path in response to the first data to provide a first propagation path delay time and an edge position for edges of signals;

testing the memory using the first propagation path delay time;

programming the plurality of non-volatile fuses to store second data;

selectively coupling one or more capacitors to the propagation path in response to the second data to provide a second propagation path delay time; and

testing the memory using the second propagation path delay time.

23. (original) The method of claim 22 wherein the memory device is a flash memory having an array of floating gate memory cells and the plurality of non-volatile fuses comprise floating gate transistors.

24. (original) The method of claim 22 further comprising:

copying the first data from the plurality of non-volatile fuses to a plurality of latches before selectively coupling one or more capacitors to the propagation path in response to the first data; and

copying the second data from the plurality of non-volatile fuses to the plurality of latches before selectively coupling one or more capacitors to the propagation path in response to the second data.

Please add new claims 25-30 as follows:

25. (new) The method of claim 15, wherein selecting edge position comprises:
selecting a single signal edge to move; and
moving the selected signal edge relative to other signal edges.

26. (new) The method of claim 15, wherein selecting edge position comprises:
selecting an edge to move;
moving the selected edge; and
moving other edges relative to the selected edge.

27. (new) The method of claim 15, wherein selecting edge position comprises:
selecting a subset of edges to move; and
moving each of the selected edges at the same time.

28. (new) The method of claim 19, wherein selecting edge position comprises:
selecting a single signal edge to move; and
moving the selected signal edge relative to other signal edges.

29. (new) The method of claim 19, wherein selecting edge position comprises:
selecting an edge to move;
moving the selected edge; and
moving other edges relative to the selected edge.

30. (new) The method of claim 19, wherein selecting edge position comprises:

selecting a subset of edges to move; and

moving each of the selected edges at the same time.